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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,473	10/30/2000	Chan-Ki Kim	P 0275255 P00H9012/US	6609

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PILLSBURY WINTHROP LLP
1600 TYSONS BOULEVARD
MCLEAN, VA 22102

EXAMINER	
JERABEK, KELLY L	

ART UNIT	PAPER NUMBER
2612	7

DATE MAILED: 04/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/698,473	KIM ET AL.	
	Examiner	Art Unit	
	Kelly L. Jerabek	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,7,8 and 13-16 is/are rejected.

7)☒ Claim(s) 3-6 and 9-12 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 October 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because in figure 2, element (61) should be element (62) and in figure 4, element (161) should be element (162). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: On page 10, line 8: "PRGECHARGE" should read "PRECHARGE".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 7-8, and 13-16 rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted Prior Art in view of Hatsuda US 5,671,181.

Re claim 1, the admitted prior art discloses in figure 1 an analog-to-digital conversion unit (30) including a double buffer block (40) that stores digital image data and outputs the data to a bit line (page 2, lines 11-20). However, the admitted prior art does not disclose an acceleration means for detecting a voltage variation of the bit line to accelerate the voltage variation of the bit line.

Hatsuda discloses in figure 10 a data read circuit used in a semiconductor storage device. The data read circuit includes a P-Channel MOSFET (951) for detecting a potential variation of a bit line (961) and a current mirror circuit (960) to accelerate the voltage variation of the bit line (col. 1, lines 52-67). This is done in order to read out the signals at a high rate (col. 2, lines 1-4). The idea of detecting a voltage variation of a bit line and accelerating the voltage variation in order to increase the read rate is well known and used in the art as suggested by Hatsuda. Therefore, it would have been obvious to include the read circuit of the semiconductor storage device including a P-channel MOSFET for detecting potential variation and a current mirror circuit as taught in Hatsuda in the analog-to-digital conversion unit of the image sensor disclosed by the admitted prior art. Doing so would provide a means for accelerating the voltage variation of a bit line and thus implementing a data read operation at a high speed.

Re claim 2, Hatsuda discloses a precharge circuit (902) for precharging the bit line (col. 1, lines 29-40).

Re claim 7, the admitted prior art discloses in figure 1 an image sensor including a pixel array (20) (page 2, lines 11-12), a control and interface means (10) (page 2, lines 11-18), a decoding means for decoding the column address signal to generate a column selecting signal (page 4, lines 25-27; page 5, lines 1-7), an analog-to-digital conversion unit (30) including a double buffer block (40) that stores digital image data and outputs the data to a bit line (page 2, lines 11-20), a ramp voltage generation means (31) for generating a ramp voltage signal (page 2, lines 11-13), a comparison means (32) for comparing a voltage level of the ramp voltage signal with the analog image data to generate a latch enable signal (page 2, lines 13-18), and a storage means (40) that stores digital image data and outputs the data to a bit line (page 2, lines 19-20). However, the admitted prior art does not disclose an acceleration means for detecting a voltage variation of the bit line to accelerate the voltage variation of the bit line.

Hatsuda discloses in figure 10 a data read circuit used in a semiconductor storage device. The data read circuit includes a P-Channel MOSFET (951) for detecting a potential variation of a bit line (961) and a current mirror circuit (960) to accelerate the voltage variation of the bit line (col. 1, lines 52-67). This is done in order to read out the signals at a high rate (col. 2, lines 1-4). The idea of detecting a voltage variation of a bit line and accelerating the voltage variation in order to increase the read

rate is well known and used in the art as suggested by Hatsuda. Therefore, it would have been obvious to include the read circuit of the semiconductor storage device including a P-channel MOSFET for detecting potential variation and a current mirror circuit as taught in Hatsuda in the CMOS image sensor disclosed by the admitted prior art. Doing so would provide a means for accelerating the voltage variation of a bit line and thus implementing a data read operation at a high speed.

Re claim 8, Hatsuda discloses a precharge circuit (902) for precharging the bit line (col. 1, lines 29-40).

Re claim 13, the disclosed prior art discloses an image sensor including a pixel array of MxN light detecting elements (page 1, lines 14-16). Each unit pixel includes a photodiode (62) and four NMOS transistors (M1, M2, M3, M4) for outputting the analog image data corresponding to the photoelectric charges (page 2, lines 23-27; page 3, lines 1-3).

Re claim 14, the disclosed prior art includes a latch enable signal that is activated to a high level while the voltage level of the ramp voltage signal is higher than that of the analog image data (page 3, lines 14-17).

Re claim 15, the disclosed prior art includes in figure 2 an image sensor with a storage means including a first NMOS transistor (M5) with a drain coupled to the digital

count signal and a gate receiving the latch enable signal, a second NMOS transistor (M6) having a drain coupled to a source of the first NMOS transistor (M5) and a gate receiving the bank selection signal, a third NMOS transistor (M7) having a source coupled to a ground and a gate receiving the digital count signal transferred via the first (M5) and second (M6) NMOS transistors, and a fourth NMOS transistor (M8) having a drain coupled to the bit line, a source coupled to a drain of the third NMOS transistor (M7), and a gate receiving the column selection signal.

Re claim 16, a PMOS transistor is turned on and a precharge operation is carried out when the clock is at a low level, therefore the phase of the clock is equal to that of the precharge signal (page 4, lines 8-12).

Allowable Subject Matter

Claims 3-6, and 9-12 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fail to anticipate or render obvious the following technical features as recited in the highlighted claims:

a. "...wherein the acceleration means includes: a first means, coupled to a node, for detecting a voltage variation of the bit line; a second means, in response to an inverted precharge signal, for determining a voltage level of the node; and a third means, responsive to the voltage level of the node, for electrically coupling the bit line to the ground" as recited in claim 3.

b. "...wherein the first means is a PMOS transistor, which has a source coupled to a power voltage level, a gate coupled to the bit line, and a drain coupled to the node" as recited in claim 4.

c. "...wherein the second means is an NMOS transistor, which has a drain coupled to the node, a source coupled to the ground, and a gate receiving the inverted precharge signal" as recited in claim 5.

d. "...wherein the third means is an NMOS transistor, which has a drain coupled to the bit line, a source coupled to the ground, and a gate receiving the voltage level of the node" as recited in claim 6.

e. "...wherein the acceleration means includes: a first means, coupled to a node, for detecting a voltage variation of the bit line; a second means, in response to an inverted precharge signal, for determining a voltage level of the node; and a third means, responsive to the voltage level of the node, for electrically coupling the bit line to the ground" as recited in claim 9.

f. "...wherein the first means is a PMOS transistor, which has a source coupled to a power voltage level, a gate coupled to the bit line, and a drain coupled to the node" as recited in claim 10.

g. "...wherein the second means is an NMOS transistor, which has a drain coupled to the node, a source coupled to the ground, and a gate receiving the inverted precharge signal" as recited in claim 11.

h. "...wherein the third means is an NMOS transistor, which has a drain coupled to the bit line, a source coupled to the ground, and a gate receiving the voltage level of the node" as recited in claim 12.

In order to expedite the prosecution of this application it is recommended that the above claims be written in independent form.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hynecek US 6,229,133 discloses an image-sensing device with delayed phase frequency modulation.

Perner et al. US 6,580,454 discloses a CMOS active pixel sensor having in-pixel local exposure control.

Denyer US 5,345,266 discloses a matrix array image sensor chip.

Aebi US 2001/0017344 discloses electron bombarded passive pixel sensor imaging.

Sohn US 2002/0085105 discloses a CMOS active pixel sensor.

Gowda et al. US 5,877,715 discloses correlated double sampling with up/down counters.

Gowda et al. US 6,115,066 discloses an image sensor with direct digital correlated sampling.

Partovi et al. US 5,508,640 discloses a dynamic CMOS logic circuit with precharge.

Frankeny et al. US 5,815,107 discloses a current source referenced high-speed analog to digital converter.

Contacts

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Kelly Jerabek whose telephone number is (703) 305-8659. The examiner can normally be reached on Monday - Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached at (703)-305-4929.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4700.

The fax number for submitting all Official communications is (703) 872-9306.

The fax number for submitting informal communications such as drafts, proposed amendments, etc., may be faxed directly to the Examiner at (703) 746-3059.

KLJ

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600